

# ABSTRACT

An objective is to perform a low power operation of a microprocessor on the pipeline stage of an instruction decode and a preceding pipeline stage without the necessity for increasing a circuit size or decoding time. An instruction code of each program for performing an instruction includes a first instruction set, which includes a flag for specifying predicate (301), and one or more second instruction sets including control specification information (302). A low power operation of each control circuit is performed for each instruction according to the instruction execution control function. Thus, without the necessity for increasing a circuit size or decoding time, it is possible to control the pipeline stage of an instruction decode and a preceding pipeline stage, achieving a low power operation of the microprocessor.